REMARKS

This paper is filed in response to the office action mailed on August 5, 2003. Because this amendment is timely filed, non extension of time fee is required.

In the office action, claims 3 and 5-9 are objected to due to a number of informalities. In response, these claims have been amended to correct the informalities.

The office action then rejects claims 1-9 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No 5,796,623 ("Butts"). In response, independent claims 1 and 6 have been amended to traverse this rejection.

Specifically, Butts discloses an apparatus and a method for performing computations, prototyping, execution and simulation using electrically reconfigurable gate arrays (ERGCA) logic chips. Thus, the reconfigurable blocks of Butts are contained in a single logic chip, *.e.g.*, a programmable gate array (PGA) (see column 7, lines 48-50). As a result, each reconfigurable block of Butts, *e.g.*, a memory block, a I/O block, a controller or the like is interconnected to each within this chip.

In stark contrast, the MCU as claimed is not contained in a single chip with the I/O block, the SFR block or the like due to the requirement of the pin connections in independent claims 1 and 6. See also figure 5, and page 6, line 11 to page 7, line 3 of the present application. An advantage of the claimed invention is that the one can test a plurality of circuits designed in accordance with specific functions separately without simultaneously testing the external I/O blocks and external pins of the MCU.

The Butts device can only be used for simulating logic circuits designed for general purposes. The Butts device cannot be used as a controller, a memory or other applications. In contrast, the test board systems of claims 1 and 6 can be used for other applications if the test board having the MCU does not have any errors.

Thus, Butts is directed toward an apparatus and a method for performing computations with electrically reconfigurable logic devices; in stark contrast, the present invention is directed toward apparatuses for supporting microprocessor development test board systems to facilitate the testing of a target board. The apparatuses of claims 1 and 6 are clearly distinct from and not anticipated by Butts and therefore applicants respectfully submit that the anticipation rejection of claims 1-9 under 35 U.S.C. § 102(b) as being anticipated by Butts is improper and should be withdrawn.

If the examiner has any further questions or comments regarding this application, he is invited to telephone the undersigned at the number listed below. An early action indicating the allowability of this application is earnestly solicited.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

Respectfully submitted,

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